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Dynamic optimum dead time in piezoelectric transformer-based switch-mode power supplies

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***Abstract*—Soft switching is required to attain high efficiency in high-frequency power converters. Piezoelectric transformer-based converters can benefit from soft switching in terms of significantly diminished switching losses and stresses. Adequate dead time is needed in order to deliver sufficient energy to charge and discharge the input capacitance of piezoelectric transformers in order to achieve zero-voltage switching. This paper proposes a method for detecting the optimum dead time in piezoelectric transformer-based switch-mode power supplies. The provision of sufficient dead time in every cycle of the switching period results in the quick start up of resonant current inside the transformer. The new method is implemented by dynamically detecting the optimum dead time for each resonant cycle and results in reduced energy loss, and consequently, increased efficiency in the converter during initialization time and steady-state operation. The theory of optimum dead time operation is also discussed in this paper. Experimental results and simulation are provided to show the implementation of the concept.**

***Index Terms*—Optimum dead time; dynamic dead time; switch-mode power supply; zero-voltage switching; piezoelectric transformer.**

NOMENCLATURE

C	Resonant capacitance of the piezoelectric transformer.
C_{d1}	Input electrode capacitance of the piezoelectric transformer.
C_{d2}	Output electrode capacitance of the piezoelectric transformer.
C_{in}	Equivalent input capacitance of the piezoelectric transformer attached to the half-bridge.
C_{oss}	Output capacitance of MOSFETs.
DT	Dead time.
HS	Switching signal driving the high-side switch.
HS_G	High-side gate-drive signal detected by ODT.
i_{res}	The resonant current of the piezoelectric transformer.
I_{pk}	Peak value of the resonant current.
L	Internal inductance of the piezoelectric transformer.
LS	Switching signal driving the low-side switch.
LS_G	Low-side gate-drive signal detected by ODT.
ODT	Optimum dead time.
R	Dielectric losses inside the transformer.
R_m	Matched load for the piezoelectric transformer.
$S(v_F)$	Switching voltage signal scaled to the voltage level of the comparator.
$S_d(v_F)$	Switching voltage signal with a slight delay.
$v_F(t)$	Switching voltage.
V_d	Voltage drop across the body diode of the MOSFETs.
Z_{HS}	Detecting a signal in the output of ODT denotes that the switching voltage has reached the positive rail.
Z_{LS}	Detecting a signal in the output of ODT denotes that the switching voltage has reached ground.
Z_{MH}	Detecting a signal in the output of ODT denotes that the switching voltage has reached the local positive peak.
Z_{ML}	Detecting a signal in the output of ODT denotes that the switching voltage has reached the local negative peak.
Φ_I	Phase shift of the resonant current with reference to the turn-off time of the low-side switch.
Φ_{ODT}	Signal phase corresponding to the optimum dead time.
ω	Switching angular frequency.

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I. INTRODUCTION

The development of piezoelectric transformer (PT)-based switch-mode power supplies (SMPS) has gathered pace in recent times due to their smaller size, lighter weight, lower cost, lower electromagnetic interference (EMI), higher power density, and higher efficiency in comparison with converters used in conventional transformers [1], [2]. Research in this area has yielded devices with greater efficiency by achieving soft switching in PT-based SMPS [1], [3], [4]. In order to obtain zero-voltage switching (ZVS), the dead time (DT) needs to be sufficiently long to allow the input capacitor of the PT to charge or discharge [5], [6]. If the DT is shorter than required, it leads to hard switching; in case the DT is longer, it can lead to hard switching or soft switching with sub-optimal efficiency [7]. Hence, a sufficiently long DT helps reduce power dissipation in switches, and consequently, this increase efficiency [8]–[10].

A fixed DT is allocated for PT-based converters with resistive matched load by analyzing the percentage of the total time required for DT. A few parameters govern the attainment of ZVS under a fixed DT: the rise in temperature, load, and changes in frequency [1], [11]. A drawback of PT-based SMPS with a fixed DT is that the length of DT needs to be separately measured for each transformer because the input capacitor of the PT is different for each transformer,

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even those from the same batch of design and production, due to the many parameters involved, e.g., oven temperature and polarization. Therefore, dynamic detection of dead time in PT-based converters is very important.

Several attempts have been made to minimize or eliminate the effect of dead time in power converters [12]–[18]. This effect is known as a distortion of the fundamental output voltage in the voltage source inverters (VSI) in pulse-width modulation (PWM) inverters [12], [13]. The relevant methods have been implemented by detecting the load current in the output of half-bridge switching, which is inapplicable to PT-based SMPS. In PT-based converters, the phase shift in the current is effected by the piezoelectric transformer. Moreover, the input capacitor of the PTs is charged or discharged during the dead time, which renders this situation different from those involving other resonant converters.

This study shows the dependence of ZVS on optional DT in piezoelectric converters, and proposes a method to detect the optimum DT for any type of PT. The outline of the remainder of this study is as follows: Section II is dedicated to a description and analysis of DT and its need in PT-based SMPS. Principle of DT is described in Subsection II-A. Furthermore, the behavior of inductorless, half-bridge, PT-based SMPS is analyzed in Subsection II-B. The idea of optimum DT is introduced in Subsection II-C and compared with prior relevant research. Following this, the implementation of the dynamic DT operation is discussed in Subsections III-A and III-B. Section IV describes experiments and simulation to show the effectiveness of the proposed method in achieving optimum DT. The final section contains the conclusions of this research.

II. Investigation and Analysis of Dead Time in PT-based Converters

A. Principle of dead time (DT)

In SMPS, switches are semiconductors with a built-in delay time. This delay time applies in the gate voltage to drive signal to start up the switching. Typically, the turn-on and turn-off delay times are not equal. Therefore, a certain amount of delay is afforded to the gate drives to prevent the simultaneous turning on of the switches [12]. Therefore, dead time is defined as the interval during a switching transition when both metal-oxide-semiconductor field-effect transistors (MOSFETs) are turned off. The dead time needs to be as short as possible to maintain an accurate low-distortion output signal in audio amplifiers [12], [19], in addition to maintaining a maximum time for switches and reducing energy loss. In PT-based SMPS, converters need to provide reactive energy to the input capacitor of the PT. However, the DT provides an appropriate interval to charge and discharge this input capacitor. In LCC resonant converters, only the output capacitances of the MOSFETs, which are typically on the order of hundreds of picofarads, should be charged by resonant current [4], [20]. However, for PT-based converters, the output capacitors of both MOSFETs and the input capacitor of the PT should be charged by resonant current to raise the voltage from 0 (V) to a positive rail V_{DC}. Fig. 1 shows an inductorless half-bridge

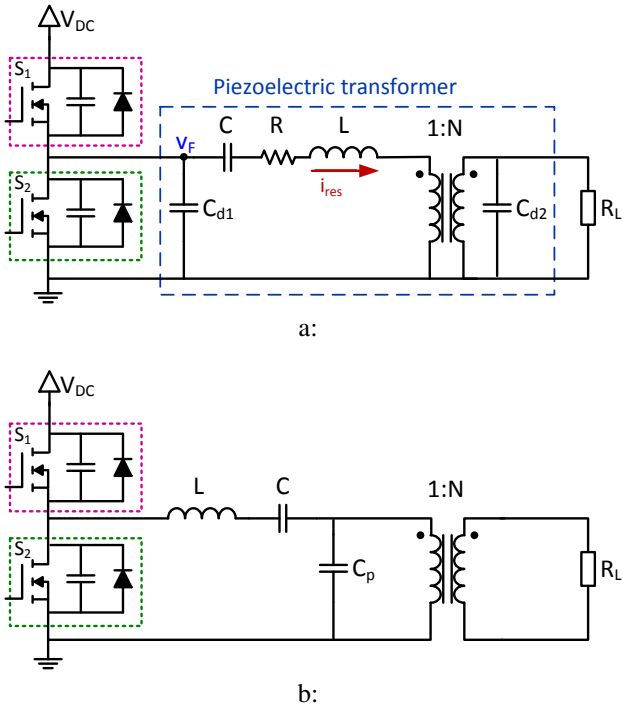

Fig. 1: a: Inductorless PT-based converter; half-bridge topology, b: LCC resonant converter.

PT-based converter [21] and an LCC resonant converter [22]. Since the input capacitance of the PTs are normally in the range of nanofarads, longer time is needed for the resonant current to provide sufficient charge to the capacitors, which means that the DT in PT-based converters is larger than that in LCC resonant converters. The challenge is to keep the DT as short as possible in order to increase efficiency. Furthermore, this will prolong the injection of energy to the transformer during the turn-on time of the high-side switch.

B. Operating modes

In the remainder of this section, the behavior of inductorless PT-based SMPS, when ZVS is attained, is discussed in detail. Eight operating modes divided into four intervals are analyzed, where each of these four intervals consists of two subintervals. Therefore, waveforms in a switching cycle are represented as $t_0 - t_{12}$. Fig. 2 shows both the switching voltage $v_F(t)$ and the resonant current i_{res} waveforms during a switching cycle in the steady state where ZVS is achieved. Time points in Fig. 2 indicate t_0: i_{res} changes direction from positive to negative values; t_2: low-side switch, S_2, is turned off; t_4: $v_F(t)$ reaches the positive rail, V_{DC}; t_5: body diode of the high-side switch, S_1, starts to conduct; t_6: high-side switch, S_1, is turned on; t_{2I}: i_{res} changes direction from negative to positive values; t_8: high-side switch, S_1, is turned off; t_{10}: $v_F(t)$ reaches to the negative rail; t_{11}: body diode of the low-side switch, S_2, conducts; t_{12}: low-side switch, S_2, is turned on. Fig. 3 shows the eight operating modes.

The following analyses are provided based on these assumptions:

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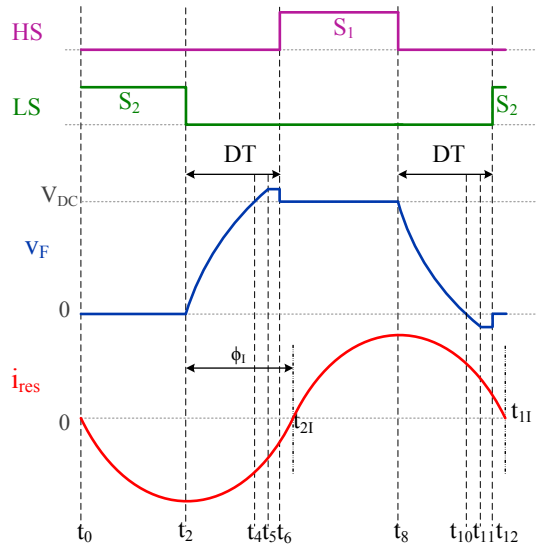

Fig. 2: Steady state switching voltage and resonant current waveforms for inductorless PT-based SMPS where ZVS is achieved.

- The converter's input capacitor is considered a summation of the input capacitance of the PT and the output capacitance of both MOSFETs: $C_{in} = 2\,C_{oss} + C_{d1}$
- Fundamental resonance due to the high quality factor of the PT.

Mason's lumped circuit is used to represent the operation of the converter in terms of resonant current and switching voltage. Resonance current is also shown in order to investigate the operating modes in detail. Since the PT behaves as a high Q-band pass filter, the resonant current is considered as the sinusoidal wave described as:

$$i_{res}(t) = I_{pk}\, sin(\omega t - \phi_I) \tag{1}$$

where I_{pk} is peak of the resonant current, ω is the angular switching frequency, and $\phi_I \in [0, \pi]$ is the current phase angle. The output capacitors C_{oss} of both MOSFET are considered in the input capacitor of the PT, since the parasitic capacitance of MOSFETs is typically considerably lower than C_{d1}. Furthermore, C_{d1} and C_{oss} are charged and discharged together in the DT. Moreover, the DT is studied in detail in this section.

1) S_2 is on: The time interval is $t_{12} - t_2$. The input capacitor of the PT is fully discharged and short-circuited through the low-side switch. At t_{12}, the low-side MOSFET is turned on, and the resonant current freewheels through the low-side switch and changes direction at t_{1I}. A minor difference in voltage occurs across the switch as the low-side switch is turned on. At t_{1I}, the value of the resonant current crosses zero and changes direction from forward to reverse. Therefore, the converter's operation spans across two subintervals. Fig. 3a and Fig. 3b show the equivalent circuit and current flow in this interval, respectively. The following equation represents the switching voltage in this interval:

$$v_F(t) = 0 \tag{2}$$

2) Both switches are off: The subinterval is $t_2 - t_5$. At t_2, the low-side switch is turned off. In this interval, both switches are off, and the resonant current retains its direction in the reverse orientation through the PT input capacitor and charges it to a voltage slightly higher than the DC-link until the diode of the high-side body starts to conduct at t_5. Fig. 3c shows the equivalent circuit and current flow in this interval. The following equation represents the waveform:

$$v_F(t) = \frac{I_{pk}}{C_{in}}\,(cos(\omega t - \phi_I) - cos(\omega t_2 - \phi_I)) + 0 \tag{3}$$

The subinterval is $t_5 - t_6$. At t_5, the high-side body diode starts conducting the reverse resonant current. Therefore, the switching voltage is limited to the sum of the diode voltage and the DC rail voltage. This interval is not required while the PT input capacitor is sufficiently charged for soft switching. Fig. 3d shows the equivalent circuit and the current flow in this interval. The voltage in this interval is expressed as:

$$v_F(t) = V_{DC} + V_d \tag{4}$$

where V_{DC} is the input voltage and V_d is the voltage drop across the body diode of the MOSFETs.

3) S_1 is on: The time interval is $t_6 - t_8$. The high-side MOSFET is turned on. The resonant current freewheels through the high-side switch and is provided to the PT. There occurs a minor voltage difference across the switch as the high-side switch is turned on. At t_{2I}, the resonant current has crossed zero and changes direction from reverse to forward. Therefore, the converter's operation is shown in two subintervals. Fig. 3e and Fig. 3f show the equivalent circuit and the current flow in this interval. The switching voltage is described as:

$$v_F(t) = V_{DC} \tag{5}$$

4) Both switches are off: The time interval is $t_8 - t_{12}$. At t_8, the high-side switch is turned off. In this interval, both switches are off. The resonant current retains its direction in the forward orientation by being fed through the PT input capacitor. Therefore, the PT input capacitor is discharged, and the voltage across approaches a value slightly below zero until the low-side body diode conducts at t_{11}. Fig. 3g shows the equivalent circuit and the current flow in this interval. The switching voltage in this interval is represented as:

$$v_F(t) = \frac{I_{pk}}{C_{in}}\,(cos(\omega t - \phi_I) - cos(\omega t_8 - \phi_I)) + V_{DC} \tag{6}$$

The time interval is $t_{11} - t_{12}$. At t_{11}, the low-side body diode begins conducting the forward resonant current. Therefore, the switching voltage is limited to a value below zero, which is equal to voltage across the body diode of the MOSFET. This time interval is undesirable while the PT input capacitor is already completely discharged. Fig. 3h shows the equivalent circuit and the current flow in this interval, where

$$v_F(t) = -V_d \tag{7}$$

C. Past research and DT optimization

As mentioned in Subsection II-A, it is important to have sufficient DT between the on times of switches. This dead time can generally be shorter or longer than required, which causes hard switching. Fig. 4 shows these situations in the steady state. In order to benefit from soft switching, DT should

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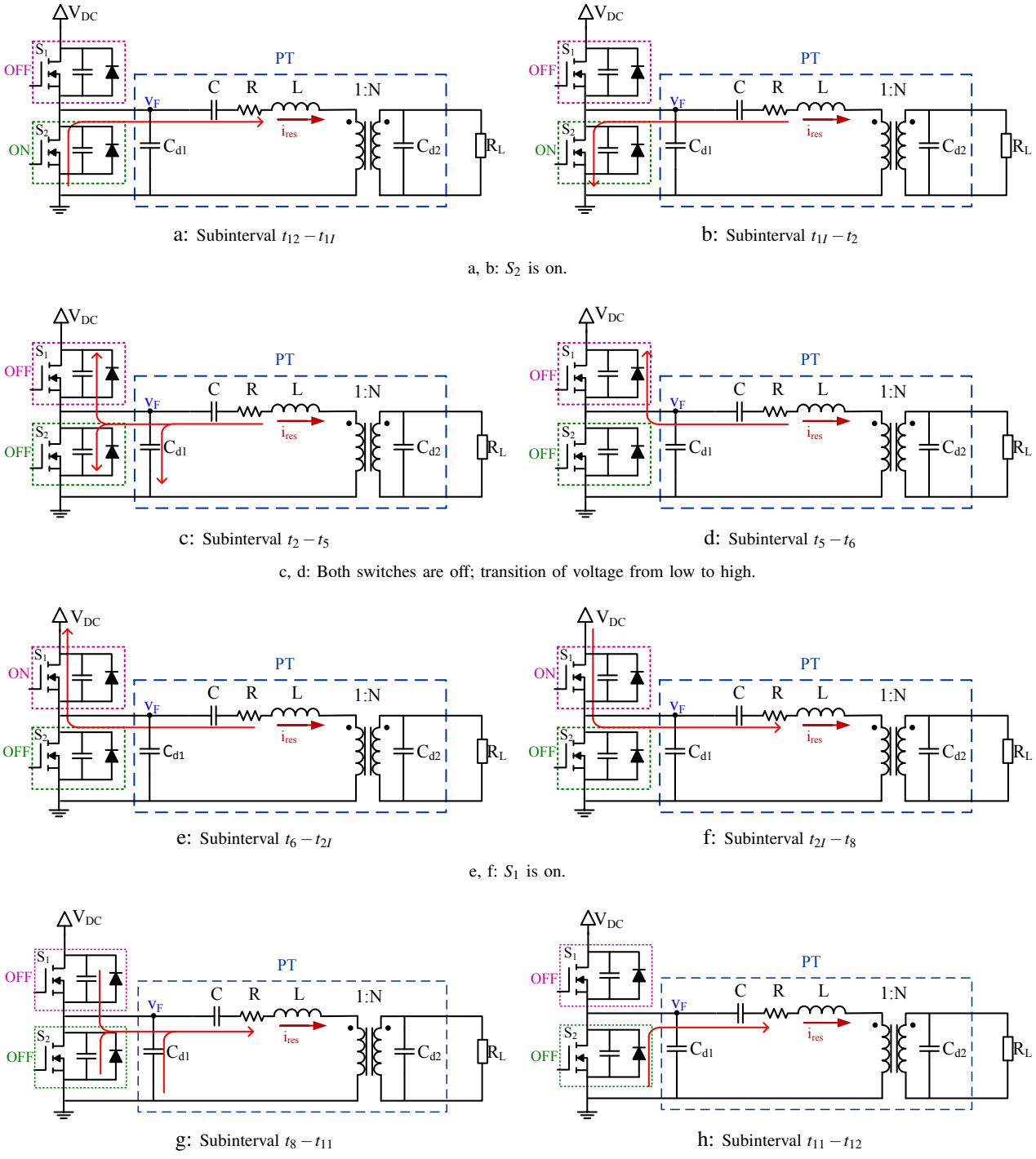

a: Subinterval $t_{12} - t_{1I}$

b: Subinterval $t_{1I} - t_2$

a, b: S_2 is on.

c: Subinterval $t_2 - t_5$

d: Subinterval $t_5 - t_6$

c, d: Both switches are off; transition of voltage from low to high.

e: Subinterval $t_6 - t_{2I}$

f: Subinterval $t_{2I} - t_8$

e, f: S_1 is on.

g: Subinterval $t_8 - t_{11}$

h: Subinterval $t_{11} - t_{12}$

g, h: Both switches are off; transition of voltage from high to low.

Fig. 3: Eight general operating modes are described for PT-based SMPS where ZVS is achieved. Mason's equivalent circuit is used for PT.

be properly applied [3].To attain ZVS, the DT should be appropriately considered to charge/discharge the input capacitor of the PT to the positive/negative rails. If switches are turned on before the input capacitor completely charges/discharges, hard switching occurs, as shown in Fig. 4a. Moreover, the case where the DT is longer than required is shown in Fig. 4b. In this case, when the resonant current changes direction, the body diodes do not conduct. Therefore, C_{d1} starts discharging at t_{2I} or charging at t_{1I} before the switches are turned on [23].

In past research, the DT was taken to be a fixed value in order to ensure that the ZVS was obtained in steady-state operation [24]–[27], and is typically sufficient. Moreover, with a fixed DT during initialization, the build up of resonant current is delayed, and it takes longer for the circuit to reach the steady state. The reduction in the start-up time may not be considerable in general, but becomes important when the

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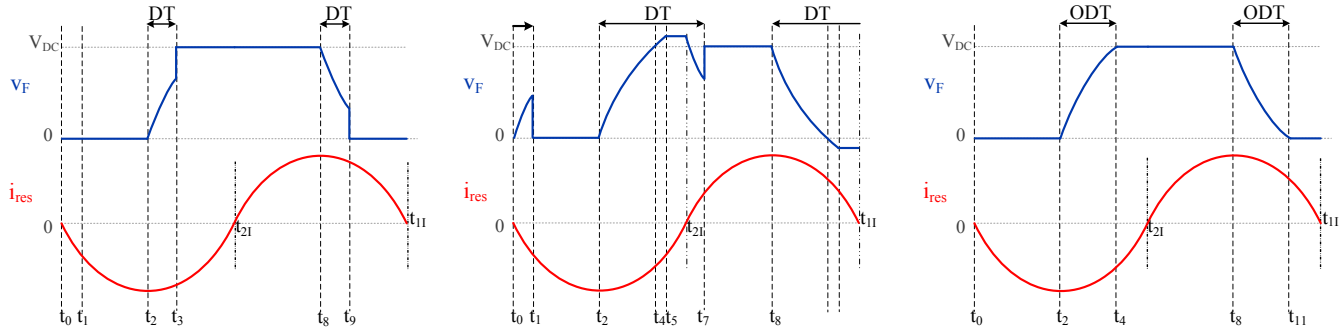

a: Insufficient dead time, short b: Insufficient dead time, long c: Optimum dead time

Fig. 4: Steady state: (a) DT is shorter than required, containing 4 operating modes. t_3 and t_9 show turn on time of S_1 and S_2, respectively. (b) DT is longer than required. t_1 and t_7 show turn on time of S_2 and S_1, respectively. (c) Switching voltage and resonant current waveforms following optimization.

converter needs to be frequently turned on and off, e.g., when burst-mode control is used to control the converter's output voltage [25], [28], [29]. In order to avoid both the cases shown in Figs. 4a and 4b and select a sufficiently long DT, the DT is optimized.

The idea implemented in this paper is to optimize dead time. In order to do so, the dead time should be detected and set dynamically in every cycle. In this method of optimization, during each switching cycle, switches are turned on when the switching voltage reaches its minimum or maximum value in start-up time, or when it reaches the positive or negative rails in the steady-state period. Fig. 4c shows waveforms when a converter in the steady state has been optimized.

D. Analysis of optimum DT

This subsection shows the dependence of optimum dead time on the resonant current, which is imposed by the resonant tank of the PT. Therefore, the switching voltage is analyzed during DT. In an inductorless PT-based SMPS, DT is partially dependent on the amount of energy that the resonant tank provides to the input capacitor of the PT [11]. Hence, when both switches are off and the input capacitor of PT starts charging/discharging, the time taken by C_{d1} to reach the rails is dependent on the instantaneous resonant current. In other words, DT is highly dependent on the peak of the resonant current, I_{pk}, and the phase angle, ϕ_I, at which the tank is operated, both of which are dependent on the PT and the load [4]. Fig. 5 shows the switching voltage and the resonant current where the optimum dead time is applied. The reference point for the phase angle is considered when low-side switch is turned off. When the low-side switch is turned off at $t_2 = 0$, negative resonant current passes through the input capacitor of the PT (C_{in}). An equivalent circuit in this operating mode is shown in Fig. 3c. $v_F(t)$ in $t_2 < t < t_4$ is described as:

$$v_F(t) = \frac{I_{pk}}{C_{in}} \left(cos(\omega t - \phi_I) - cos(\phi_I)\right) \tag{8}$$

By implementing ODT, $v_F(t_4) = V_{DC}$ and $\omega t_4 = \phi_{ODT}$, the analysis of ODT yields

$$\phi_{ODT} = \arccos\left(\frac{V_{DC}\, C_{in}}{I_{pk}} + cos(\phi_I)\right) + \phi_I \tag{9}$$

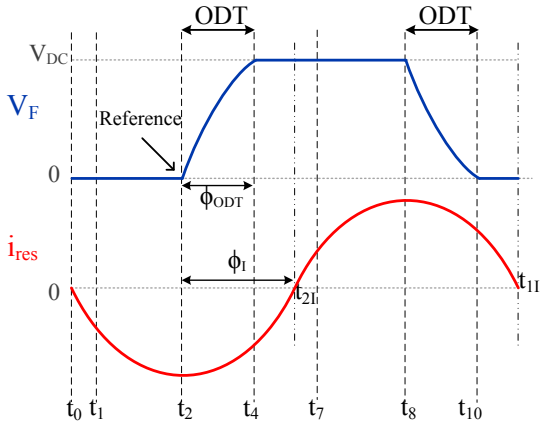

Fig. 5: Switching voltage and resonant current with ODT.

where $\phi_{ODT} \in [0, \pi]$. The dependence of the ODT on resonant current (I_{pk} and ϕ_I) shows that it is difficult to analytically calculate the ODT, even for a specific PT and a specific load. However, the amplitude of the resonant current and its phase angle varies with the temperature of the PT [30]. The method proposed in this paper to detect the ODT is a simple solution that works by varying the temperature and load of the PT.

III. Optimum Dead Time (ODT)

A. Dynamic DT operation

As shown in Fig. 2, there are two DT periods in each switching cycle corresponding to time intervals $t_2 - t_6$ and $t_8 - t_{12}$, as described in Subsection II-B. Having two subintervals $t_2 - t_4$ and $t_8 - t_{10}$ is necessary in order for the voltage to reach across C_{d1} to the rails to attain ZVS. In effect, optimum DT is defined as the minimum time required for the switching voltage ($v_F(t)$) to reach from one DC rail voltage to another. Therefore, by detecting time points where the switching voltage reaches zero and the positive rails, time intervals $t_4 - t_6$ and $t_{10} - t_{12}$ can be reduced to the minimum possible. On the contrary, optimizing time intervals $t_2 - t_4$ and $t_8 - t_{10}$ occurs by detecting t_4 and t_{10}, shown in Fig. 2, in order to turn on the high-side and low-side switches at these time points, respectively. This yields optimum dead time. The ODT leads to a quick start up of the resonant current by maximizing the on time of switches to

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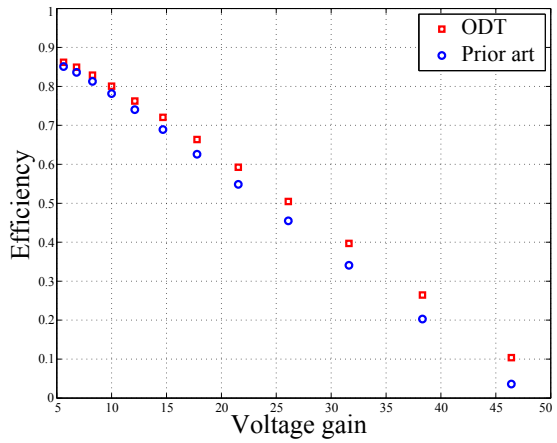

Fig. 6: Efficiency increment by applying ODT for the step-up converter with capacitive load compated to the past research [25], [26].

energize the resonant tank and build up the resonant current. This consequently increases the converter's efficiency.

Improvement in efficiency by applying the ODT for the step-up converter with a capacitive load is shown in Fig. 6. Fig. 7 shows the DT period by waveform and an equivalent circuit of the inductorless PT-based converter. The load was considered the PT's resistive matched load with the relation

$$R_m = \frac{1}{\omega C_{d2}} \tag{10}$$

In a DT interval, the PT's input capacitor was charged/discharged. In order to obtain the shortest period for switching voltage $v_F(t)$ to reach the DC-link in the DT interval, a novel idea was proposed and implemented in this paper. For example, the DT interval during which C_{in} is charged $(t_2 - t_6)$ is explained in detail. At the start of the DT interval, the resonant current has a negative value but its amplitude is dependent on the phase shift imposed by the transformer. For simplicity of understanding, the best case is explained in this section in detail, where $\phi_I = \pi/2$. If $ODT > \pi/2\omega$, the resonant current changes its direction from negative to positive, and causes the discharge of C_{in} in order to provide energy back to the resonant tank, as shown in Fig. 7e. If the energy of the resonant tank is supplied through the DC-link by turning on the high-side switch, it prevents C_{in} from being discharged (Fig. 7f). If C_{in} is not discharged in $t_2 - t_6$ or charged in $t_8 - t_{11}$,

- Lower switching losses, since $\Delta V_{F_b} < \Delta V_{F_a}$. This results in higher efficiency.
- More energy injected to the PT for the build up of the resonant current to reach the steady state. This causes resonant current of higher amplitude in each cycle as well as shorter start-up time. The following shows the parameterized energy saved by applying ODT:

$$\Delta E = \Delta E_b - \Delta E_a \tag{11a}$$

where,

$$\Delta E_b = \frac{1}{2} C_{in} V_{DC}^2$$

$$\Delta E_a = \frac{I_{pk}^2}{4 C_{in}} \left[\Delta DT + \frac{1}{2} sin(2\Delta DT) \right] \tag{11b}$$

B. Implementation of the proposed method

By measuring input voltage of the PT and comparing it with the rail voltages (zero/positive), the switches should be turned on, which is satisfactory for the steady-state period. The start up time or the initialization time specifies the period from when the converter turns on to when the resonant current in the PT reaches the maximum amplitude in its operating point. In this period, the resonant current increases continuously but does not reach the highest possible amplitude. Therefore, the input capacitor is not charged up to the positive rail or discharged down to zero. Fig. 9 shows the states that may occur for the voltage and current waveforms in the initialization period. Accordingly, the two states may occur during the DT in the start up. In one case, the switching voltage may pass through the local maximum/minimum before switches are turned on. Fig. 9b shows the switching voltage and the resonant current for this case. Extrema occur in $v_F(t)$ because the resonant current changes its direction during the dead time. Therefore, it causes the input capacitor to charge and discharge.

In the other case, the switching voltage continues to increase/decrease until the switches are turned on. This means that the switching voltage will not pass through any local extrema. In this case, the amplitude of the resonant current is not sufficiently high to charge the input capacitor. This situation is shown in Fig. 9a. In the meantime, the resonant current changes direction during a switching cycle. The difference between the cases, which may originate in the start-up period, is the amplitude of the resonant current. The resonant current starts to build up once the converter is turned on, and grows in amplitude until it reaches the steady state. In the steady state, the amplitude of the resonant current is constant under the same conditions, i.e., input voltage, temperature, and load. At the beginning of the initial period, the amplitude of the resonant current is very low. Hence, there is insufficient energy injected into the input capacitor of the PT during the dead time to charge the C_{in} to the DC-link voltage. Both cases are shown in Fig. 9a and Fig. 9b. The best condition for the charge of C_{in} is shown in Fig. 9c, where the resonant current is near its peak when the dead time starts, and this means that $\phi_I = \pi/2$ is related to $t_2 = 0$. Therefore, $v_F(t)$ can be simplified as:

$$v_F(t) = \frac{I_{pk}}{C_{in}} sin(\omega t) \tag{12}$$

Consequently, the total amount of energy provided to C_{in} during dead time is defined as $\Delta t = t_6 - t_2$.

$$\Delta E = \frac{1}{2} C_{in} V_{F(rms)}^2 |_{\Delta t} = \frac{I_{pk}^2}{4 C_{in}} (1 - \frac{1}{2\omega\Delta t} sin(2\omega\Delta t)) \tag{13}$$

Therefore, it is important to turn on switches at the zero crossing of the resonant current, as shown in Fig. 9c. Consequently, in order to optimize dead time either in the initialization state or in the steady state, switches should be turned on when the switching voltage reaches the rails (positive/ zero) or resonant current crosses zero. If none of these signals are detected, the

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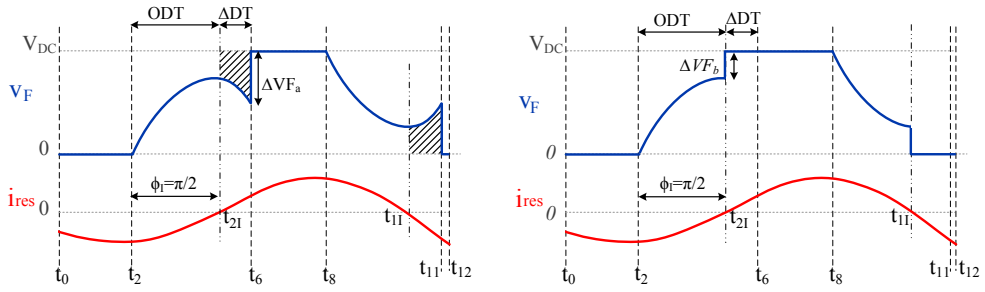
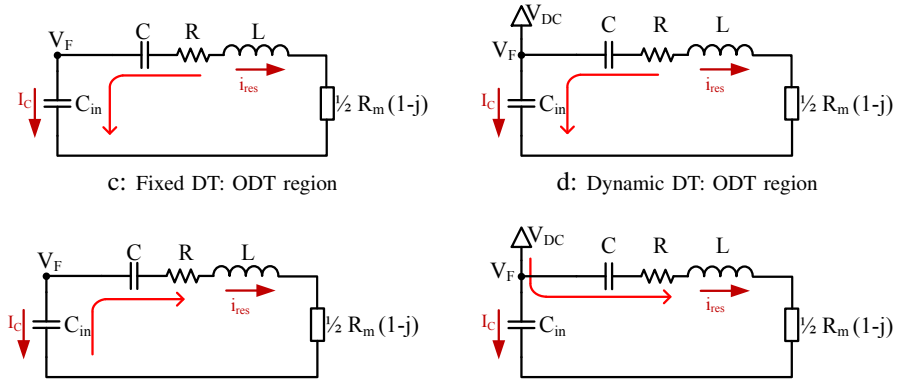


a: Fixed DT b: Dynamic DT

a, b: Resonant current and switching voltage waveforms.



c: Fixed DT: ODT region d: Dynamic DT: ODT region

e: Fixed DT: ΔDT region f: Dynamic DT: ΔDT region

c, d, e, f: Equivalent circuits in DT interval for case a: (c and e) and case b: (d and f); R_m is matched load.

Fig. 7: Effect of dynamic dead time in reducing requisite input energy and switching losses in initialization time.

circuit applies a fixed DT to facilitate the build up of resonant current. Since there is no direct access to the resonant current inside the PT, the switching voltage is used as a reference for detecting the DT in this implementation. Table I shows both cases during the initialization period. Fig. 8 shows a block diagram of the converter used in this paper. Outputs of the ODT block determine turn on time of the high-side and low-side switches.This contribution is performed dynamically by mix of analog and digital control techniques used in digital block and programming done in field-programmable gate array (FPGA). FPGA is used for implementation of control techniques to generate high-side and low-side gate voltages based on the detected signals in the output of the ODT block.

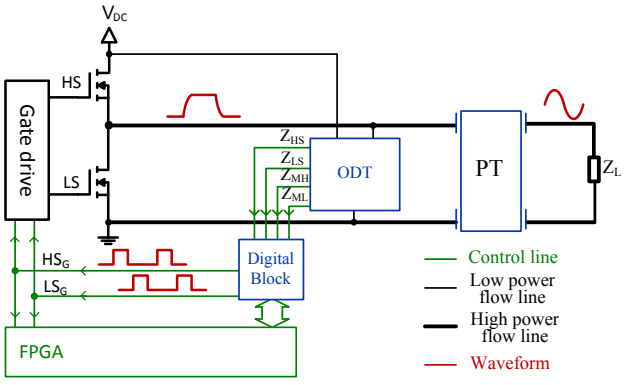


Fig. 8: Block diagram of converter with ODT and mix of analog and digital control techniques through digital block and FPGA.

C. ODT circuit description

Fig. 10 shows a circuit block diagram of the implemented optimum DT. The circuit consists of two parts: the "steady state ODT detector" detects the ODT in the steady state, and the "extrema detector" identifies the ODT during the initialization period. For the steady state, the switching voltage is compared to the positive DC-link (V_{DC}) and the zero line through op-amps 1 and 2. This results in Z_{HS} and Z_{LS} in the output of the ODT block. Therefore, the high- and low-side switches are turned on by raising the edges of Z_{HS} and Z_{LS} in the steady state. For the initialization period, the switching voltage taken as the input signal S is compared with its delayed S_d. The local maximum is detected when $S_d > S$ and the local minimum is detected when $S > S_d$. A voltage range called the middle range (M) is defined between V_{Low} and V_{Hi}. It is considered 10% and 90% of V_{DC}, respectively, in order to define a margin for local extrema detection. This also prevents the influence of noise in extrema detection. Op-amps 3 and 4 determine whether the $v_F(t)$ is above V_{Low} or below V_{Hi}. The amplitude of $v_F(t)$ is scaled down and called as signal S. A high-precision dual output comparator is used to compare $v_F(t)$ known as signals S with its delayed signal S_d. The outputs of the ODT block are controlled by the digital block. The high-side MOSFET is turned on when Z_{HS} or Z_{MH}

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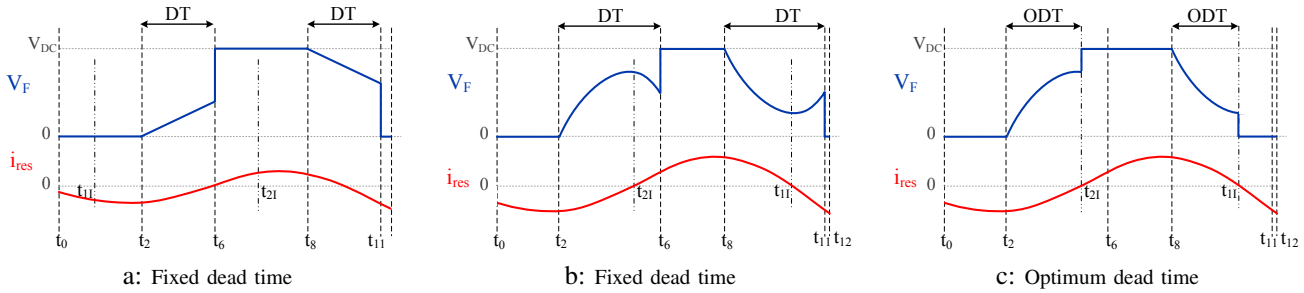
TABLE I: SWITCHING VOLTAGE COMPARISON BETWEEN PAST RESEARCH AND OPTIMUM DEAD TIME METHOD

State	Prior art	Optimum dead time
Initialization time	DT longer than required DT shorter than required	Sufficient DT
Steady state	Sufficient DT; not optimized	Sufficient DT



a: Fixed dead time b: Fixed dead time c: Optimum dead time

Fig. 9: Start-up period with fixed DT for (a) and (b). Switching voltage does not reach the rails. The resonant current is low in amplitude. (a) The PT's input capacitor charges/discharges slowly. (b) $v_F(t)$ reaches a local extrema. (c) The ODT is applied to the start up to detect extrema.

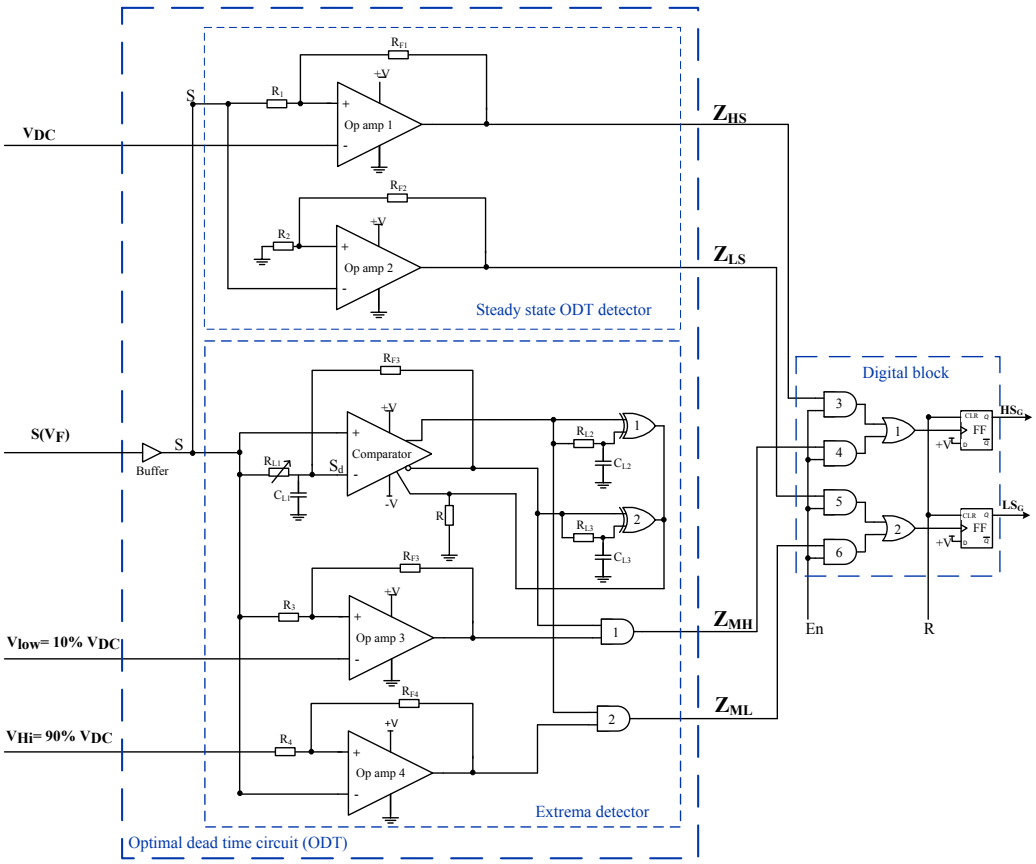


Fig. 10: Circuit block diagram of ODT.

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TABLE II: SWITCHING TURN ON TIME POINTS

	Prior art	Optimization
Start up time	Fixed DT	Switching voltage reaches its extrema
Steady state	Fixed DT	Switching voltage reaches the rails

digitally becomes '1', and the low-side MOSFET is turned on when Z_{LS} or Z_{ML} becomes '1'. The control signal reset "R" turns off the switches once the allocated on time ends. However, "En" enables/disables the contribution of the ODT to the converter. Voltages V_{DC}, V_{Hi}, and V_{Low} are scaled to the voltage level of the comparator's input. The Boolean functions implemented for the outputs of the ODT are:

$$\begin{cases} Z_{ML} = (S < V_{Hi}) \cdot (S > S_d) \\ Z_{MH} = (S > V_{Low}) \cdot (S < S_d) \\ Z_{HS} = (S > V_{DC}) \\ Z_{LS} = (S < 0) \end{cases} \tag{14}$$

$$\begin{cases} HS_G = (Z_{HS} + Z_{MH}) \cdot En \cdot \overline{R} \\ LS_G = (Z_{LS} + Z_{ML}) \cdot En \cdot \overline{R} \end{cases} \tag{15}$$

Furthermore, the functionality of the ODT block is shown through waveforms both in the steady state and the start-up time. Fig. 11 shows the signal waveforms in the start-up period related to Fig. 9c. Fig. 12 shows the signal waveforms for the steady state related to Fig. 4c.
Table I compares the ODT with the results of past work by providing a demonstration of switching voltage waveforms both during start up and in the steady state. Table II compares the switching voltage values from past research and the ODT.

IV. Results

The experiments and simulation to establish the effectiveness of the proposed method were carried out by using a radial-mode piezoelectric transformer shown in Fig. 13, and with an equivalent circuit shown in Fig. 1a. The parameter values of the PT are shown in Table III. The PT resonant frequency was 116.3 kHz for the simulation with a resistive load of 300 Ω.Fig. 14 shows the simulation results in start-up transient time both for prior art [25] and for optimization state. By implementing optimum DT, a shorter initialization time was achieved in comparison with the results of past work. The top subfigure of Fig. 14 shows the result for a fixed DT chosen very close to the ODT in the steady state. The selected fixed DT shows almost the best case of setting the DT in past work in the area. The switching voltage V_F reaches the positive rail in the eighth cycle. The bottom subfigure shows the simulation results by applying dynamic DT to each switching cycle. The switches are turned on by detecting the extrema of the switching voltage during start up. The switching voltage reaches the positive rail in the sixth cycle. A comparison of these two cases establishes the idea that the converter reaches the steady state more quickly by applying the ODT. Fig. 15 shows the board that was designed and used for the experiment.

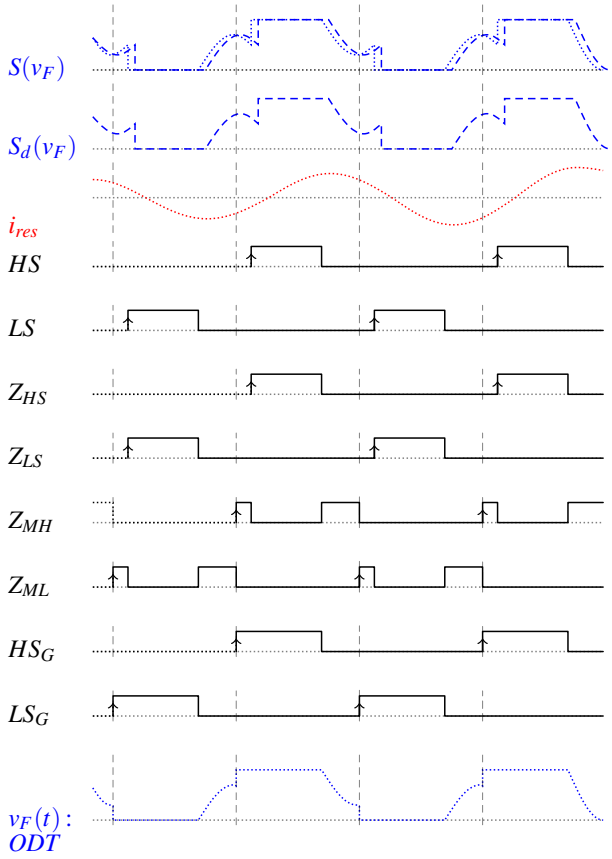

Fig. 11: Signal waveforms, in the start-up, Z_{MH} and Z_{ML} turn on the S_1 and S_2 switches, respectively.

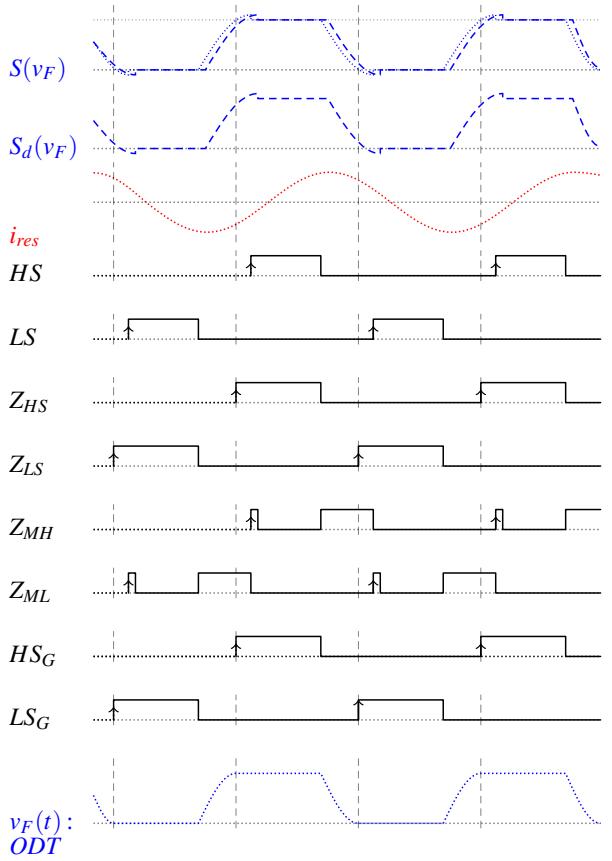

Fig. 12: Signal waveforms, in the steady state when ZVS is achieved; Z_{HS} and Z_{LS} turn on the S_1 and S_2 switches, respectively.

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TABLE III: PT EQUIVALENT PARAMETERS

Parameter	Value	Parameter	Value
C_{d1}	3.8 nF	C_{d2}	626 pF
C	565 nF	R	5.6 Ω
L	3.5 mH	N	3.5

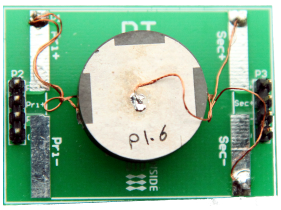


Fig. 13: The Radial-mode piezoelectric transformer used in experiments.

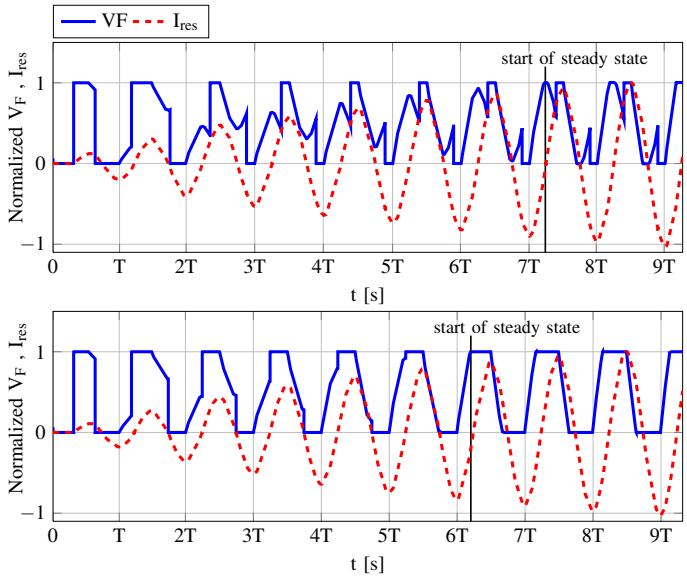


Fig. 14: Start-up period: Comparison of results of past work (top plot) with a fixed DT with the ODT (bottom plot). The driver reaches the steady state faster with ODT than previously proposed methods.

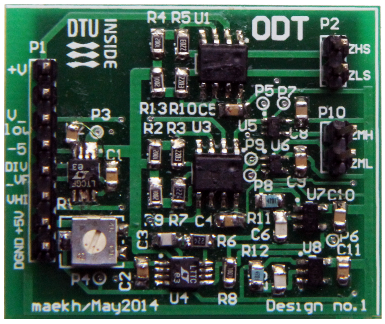
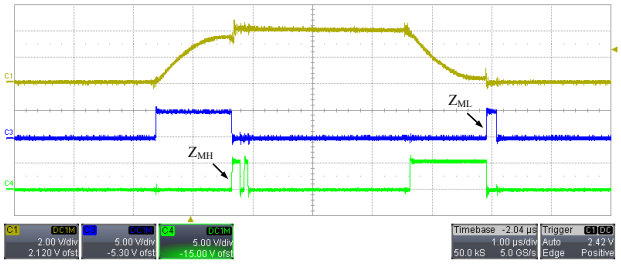
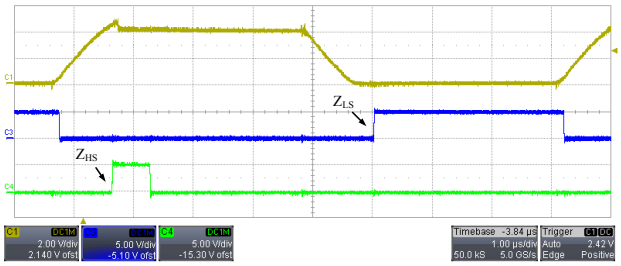


Fig. 15: ODT board used for experiments.



a: Local minimum/maximum detection of switching voltage ($v_F(t)$) in the start-up period or when hard switching occurs; C1: switching voltage $v_F(t)$, C3: local minimum detector by signal Z_{ML}, C4: local maximum detector by signal Z_{MH}.



b: Switching voltage $v_F(t)$ in the steady state or when soft switching occurs. C1: switching voltage $v_F(t)$, C3: negative rail detector by signal Z_{LS} , C4: positive rail detector by signal Z_{HS}.

Fig. 16: Outputs of ODT block by detecting optimum dead time.

Fig. 16 shows the experimental results. In the result shown, input voltage is 4 V with a load of 300 Ω. The measurement is done in low voltage due to limitation of PT in terms of its power transfer capability. The implementation can be used for every input voltage if the desired power can be put through the PT. Fig. 16a shows waveforms at 118.7 kHz, when the ODT block detected an extrema, and Fig. 16b shows waveforms at 119.2 kHz, when the switching voltage reached the rails. A slight delay can occur from the time when the ODT is detected until the switches are turned on due to propagation delay in the gate driver. This time delay can be reduced by selecting a gate driver with lower propagation delay. In this setup, the propagation delay of the gate driver was 35 ns.

V. Conclusion

This paper dealt with the theory of dead time along with its necessity in resonant converters, particularly in inductorless PT-based SMPS. Moreover, the importance of selecting an appropriate dead time in order to avoid hard switching was explained. A new method was proposed and implemented to detect the optimum dead time in PT-based SMPS. However, this method can generally be used for any PT-based converter, even though it is implemented in an inductorless PT-based SMPS. The optimum dead time is obtained at any switching frequency and is updated during every cycle. Detecting the optimum dead time yields two advantages for power converters: reducing the start-up time of the converter in transient operation, and maximizing the turn-on time of switches in the steady state. Furthermore, experimental results and a simulation verified the effectiveness of the proposed method. The ODT is used due to its effective build up of resonant current through an optimized start up, minimization of dead time, the outstanding performance of the ZVS, and energy conservation during initialization. This results in greater efficiency.

A major disadvantage of using ODT is its complex control method, since an additional ODT block is required to be added to the converter. Furtheremore, mixed analog and digital control techniques are needed to impose output signals of the ODT block into the gate voltages in every switching cycle.

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